IN THE CLAIMS

Claim 1 (Currently Amended): A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising ~~the steps of~~:

~~(A)~~ preparing a power-on mode for performing a DRAM operation by controlling a threshold voltage of the transistor; and

~~(B)~~ preparing a power-off mode for storing a data included in the capacitor into the floating gate.

Claim 2 (Currently Amended): The method as recited in claim 1, wherein the ~~step (A)~~ preparing the power-on mode includes ~~the steps of~~:

~~(A-1)~~ moving the data stored in the floating gate into the capacitor; and

~~(A-2)~~ adjusting ~~a~~the threshold voltage of the transistor in all of the memory cells to a first threshold voltage.

Claim 3 (Cancelled).

Claim 4 (Currently Amended): The method as recited in claim 2, wherein the ~~step (A-1)~~ moving the data includes ~~the steps of~~:

~~(A-1-a)~~ charging the capacitors of all memory cells with a logic HIGH datum; and

~~(A-1-b)~~ discharging the capacitor in the memory cell having the transistor, its floating gate storing a logic high datum.

Claim 5 (Currently Amended): The method as recited in claim 4, wherein the step ~~(A-1)~~moving the data includes ~~the step of (A-1-c)~~ refreshing the plurality of capacitors.

Claim 6 (Currently Amended): The method as recited in claim 5, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the ~~step (A-1)~~moving the data is carried out in a row-by-row basis.

Claim 7 (Currently Amended): The method as recited in claim 6, wherein the ~~step (A-1-a)~~charging the capacitors includes ~~the steps of~~:

~~(A-1-a-1)~~ supplying one word line connected to a multiplicity of the memory cells with a first threshold voltage in order to turn on the transistors in all of the memory cells;

~~(A-1-a-2)~~ writing the logic HIGH datum in the capacitors of the memory cells coupled to the word line; and

~~(A-1-a-3)~~ repeating the ~~steps (A-1-a)~~charging the capacitors and ~~(A-1-b)~~ discharging the capacitor in the memory cell having the transistor until all of the capacitors in the plurality of the memory cells are charged with the logic HIGH datum.

Claim 8 (Currently Amended): The method as recited in claim 4, wherein the ~~step (A-1-b)~~ discharging the capacitor in the memory cell having the transistor includes ~~the steps of~~:

~~(A-1-b-1)~~ supplying all of the word lines with a second threshold voltage in order to turn~~ing~~ on the transistors, its floating gate storing the logic HIGH datum; and

~~(A-1-b-2)~~ supplying all of the bit lines with about 0 V in order to ~~discharging~~ discharge the capacitors in the memory cell having the transistor, its floating gate storing the logic HIGH datum.

Claim 9 (Currently Amended): The method as recited in claim 2, wherein the ~~step (A-2)~~ adjusting the threshold voltage includes ~~the steps of~~:

~~(A-2-a)~~ supplying all gates of the transistors in all of the memory cells with a first predetermined voltage in order for fulfilling electrons in the floating gate;

~~(A-2-b)~~ charging all of the capacitors in all of the memory cells; and

~~(A-2-c)~~ decreasing the threshold voltage of the transistors to the first threshold voltage.

Claim 10 (Currently Amended): The method as recited in claim 9, wherein the adjusting the threshold voltage ~~step (A-2)~~ including ~~the steps of~~:

~~(E)~~ backing up the captured data in the capacitor before the ~~step (A-2-a)~~supplying all gates; and

~~(F)~~ restoring the backup data in the capacitor after the ~~step (A-2-c)~~decreasing the threshold voltage.

Claim 11 (Currently Amended): The method as recited in claim 10, wherein the ~~step (A-2-b)~~ charging all of the capacitors includes ~~the steps of~~:

~~(A-2-b-1)~~ supplying one side of the capacitor with about 0 V; and

~~(A-2-b-2)~~ supplying the bit line with the logic HIGH datum.

Claim 12 (Currently Amended): The method as recited in claim 11, wherein the decreasing the threshold voltage ~~step (A-2-c)~~ includes ~~the steps of~~:

~~(A-2-c-1)~~ removing electrons in the floating gate of the memory cells;

~~(A-2-c-2)~~ discharging the capacitor by supplying the gate of the transistor in the memory cells with the first threshold voltage; and

~~(A-2-c-3)~~ repeating the ~~steps (A-2-c-1)~~ removing electrons ~~to~~ and ~~(A-2-c-2)~~discharging the capacitor by supplying the gate until all of the capacitors ~~is~~ are discharged.

Claim 13 (Currently Amended): The method as recited in claim 12, wherein the ~~step (A-2-c-1)~~ removing electrons includes ~~the steps of~~:

~~(A-2-c-1-a)~~ supplying a gate of the transistor in all of the memory cells with a negative voltage;

~~(A-2-c-1-b)~~ supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

~~(A-2-c-1-c)~~ moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

Claim 14 (Currently Amended): The method as recited in claim 13, wherein the ~~step (A-2-c-2)~~moving electrons in the floating gate includes ~~the steps of~~:

~~(A-2-c-2-a)~~ supplying the gate of the transistor with a second threshold voltage; and

~~(A-2-c-2-b)~~ discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold voltage.

Claim 15 (Currently Amended): The method as recited in claim 14, wherein the ~~step (A-2)~~ adjusting the threshold voltage includes the ~~step of (A-2-d)~~ refreshing all of the memory cells.

Claim 16 (Currently Amended): The method as recited in claim 15, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines

and bit lines and the adjusting the threshold voltage~~step (A-2)~~ is carried out in a row-by-row basis.

Claim 17 (Original): The method as recited in claim 13, wherein the capacitor is a coupling capacitor.

Claim 18 (Currently Amended): The method as recited in ~~claim 3~~claim 1, wherein the ~~step (B-1)~~ preparing the power-off includes~~ the steps of~~:

~~(B-1-a)~~ removing electrons in the floating gate of the memory cell storing a logic HIGH datum;

~~(B-1-b)~~ discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage; and

~~(B-1-c)~~ repeating the ~~steps (B-1-a)~~removing electrons in the floating gate of the memory cell storing a logic HIGH datum ~~to~~ and ~~(B-1-b)~~ removing electrons in the floating gate of the memory cell storing a logic HIGH datum until all of the capacitors ~~is~~ are discharged.

Claim 19 (Currently Amended): The method as recited in claim 18, wherein the ~~step (B-1-a)~~ removing electrons in the floating gate of the memory cell storing a logic HIGH datum includes the steps of:

~~(B-1-a-1)~~ supplying a gate of the transistor in all of the memory cells with a negative voltage;

~~(B-1-a-2)~~ supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

~~(B-1-a-3)~~ selectively moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

Claim 20 (Currently Amended): The method as recited in claim 18, wherein the ~~step (B-1-b)~~ discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage includes ~~the steps of~~:

~~(B-1-b-1)~~ supplying the gate of the transistor with a second threshold voltage; and

~~(B-1-b-2)~~ discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold voltage.

Claim 21 (Currently Amended): The method as recited in claim 20, wherein the ~~step (B-1-b)~~ discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage includes ~~the steps of (B-1-b-c)~~ refreshing the memory cell.

Claim 22 (Currently Amended): The method as recited in claim 21, wherein the ~~step (B-1-b)~~ discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage is carried out row-by-row.

Claim 23 (Original): The method as recited in claim 19, wherein the capacitor is a coupling capacitor.

Claim 24 (Currently Amended): The method as recited in claim 2, wherein the ~~step (A-1)~~ moving the data further includes ~~the step of~~:

~~(A-1-a)~~ supplying a word line with a voltage defined by the following equation:

$$V_{wl} = V_{blp} + (V_{th-H} + V_{th-L})/2$$

where V_{blp} is a bit line precharge voltage, V_{th-H} is a first threshold voltage, and V_{th-L} is a second threshold voltage; and

~~(A-1-b)~~ writing logic HIGH or LOW data in the capacitor in response to whether the threshold voltage is the V_{th-H} or the V_{th-L}.

Claim 25 (Currently Amended): The method as recited in claim 23, wherein the step moving the data~~(A-1)~~ includes ~~the step of (A-1-c)~~ refreshing the plurality of memory cells by supplying each word line with a voltage level being higher than the logic HIGH datum.

Claim 26 (Currently Amended): The method as recited in claim 25, wherein the moving the data~~step (A-1)~~ is carried out row-by-row.

Claim 27 (Currently Amended): The method as recited in claim 26, wherein the ~~step (A-1-a)~~ supplying a word line further includes ~~the step of (A-1-a-1)~~ supplying other word lines with a predetermined negative voltage except for the word line supplied with the 'V_{wl}'.

Claim 28 (Currently Amended): A non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells in a matrix, each memory cell comprising:

a capacitor for storing a data; and

a transistor for transmitting the data stored in the capacitor to a bit line, wherein the transistor includes a drain, a source, and a gate having a control gate and a floating gate for storing the data when a power is off and a threshold voltage of the transistor is controlled when the power is on,

wherein one terminal of the capacitor is coupled to the drain of the transistor and the other terminal of the capacitor is supplied with a controllable voltage determined according to an operation mode.

Claim 29 (Previously Presented): The NVDRAM device recited in claim 28, wherein the floating gate of the transistor is made of nitride.

Claim 30 (Previously Presented) The NVDRAM device recited in claim 29, wherein the floating gate of the transistor formed in a single layer serves as a data storage.

Claim 31 (Currently Amended): A non-volatile dynamic random access memory (NVDRAM) including a plurality of memory cells in a matrix, wherein each memory cell includes:

a control gate layer coupled to a word line;

a capacitor for storing data; and

a floating transistor for transmitting the stored data in the capacitor to a bit line and storing the data therein in response to an operation mode, wherein a threshold voltage of the floating transistor is controlled when the power is on,

wherein one terminal of the capacitor is coupled to a drain of the floating transistor and the other terminal of the capacitor is supplied with a controllable voltage determined according to the operation mode.

Claim 32 (Original): The NVDRAM device as recited in claim 31, wherein the control gate layer is made of metal and the gate of the floating transistor is made of nitride.

Claim 33 (Original): The NVDRAM recited in claim 32, wherein the gate of the floating transistor formed in a single layer serves as a data storage.